Time: 20 Minutes (upload time 5 minutes)

I will not accept a paper if you fail to upload it on time.

Name:

Registration Number:

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| 1. | Design a transistor-level schematic for a compound CMOS logic gate for the following function:  Y = (A . B + C . D)  Briefly explain each step. | 10 | CO2 |
| 2. | Briefly explain the input output procedure of the following circuit. Mention the specialty of this circuit. | 10 | CO2 |